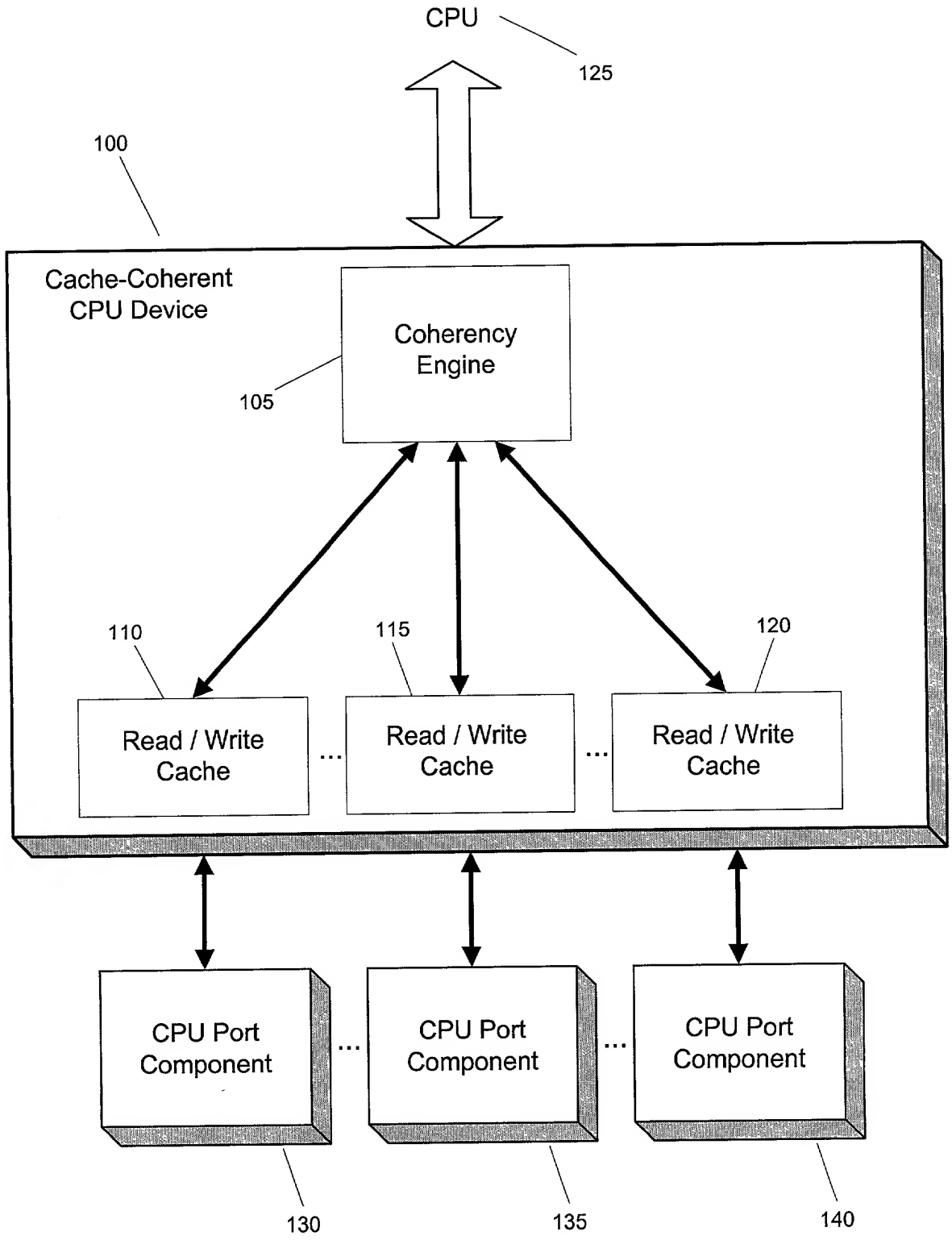
CPU
125
100
Cache-Coherent
CPU Device
Coherency
Engine
105
110
115
120
Read / Write
Cache
Read / Write
Cache
Read / Write
Cache
CPU Port
Component
CPU Port
Component
CPU Port
Component
130
135
140

Fig. 1

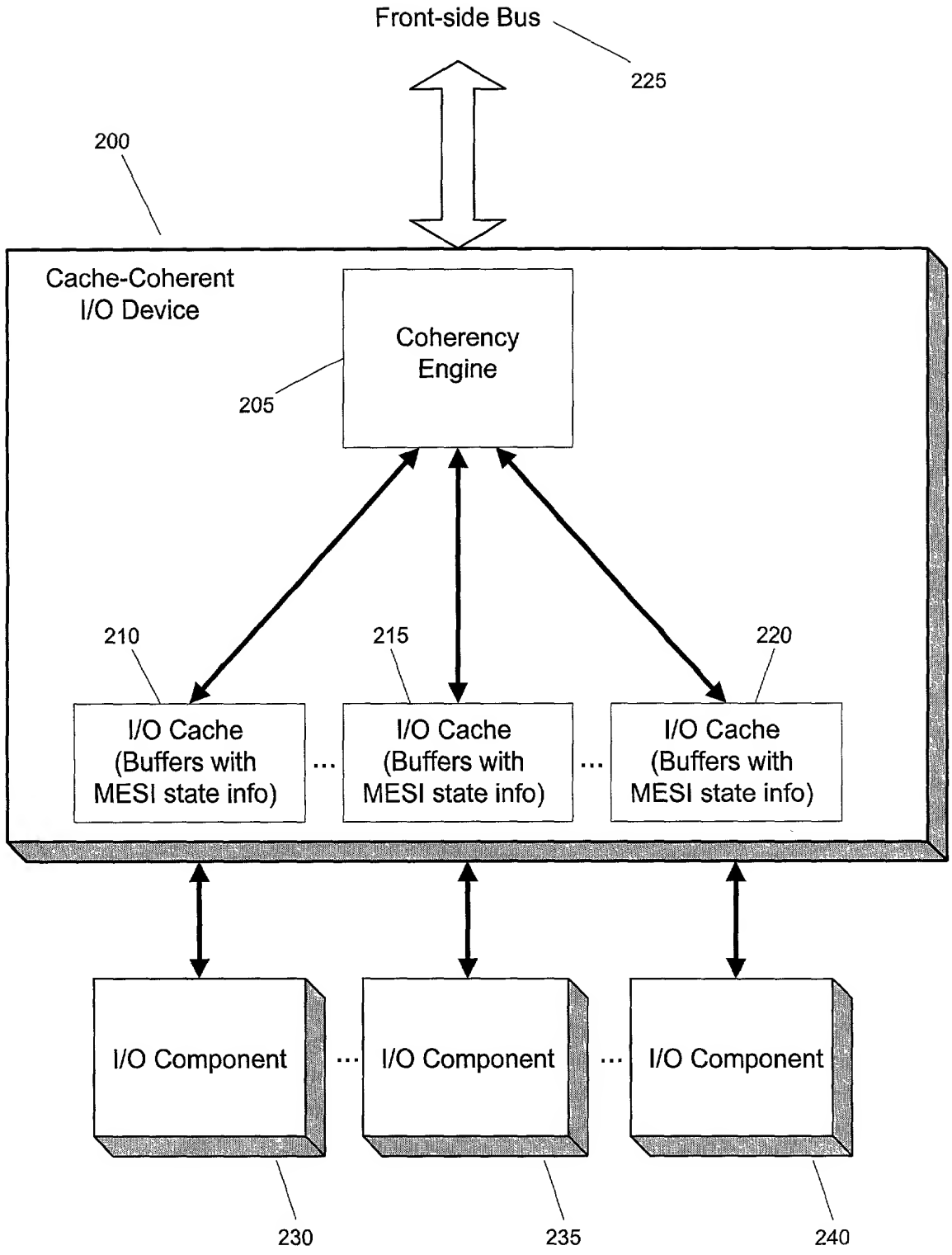
Front-side Bus
225
200
Cache-Coherent
I/O Device
Coherency
Engine
205
210
215
220
I/O Cache
(Buffers with
MESI state info)
I/O Cache
(Buffers with
MESI state info)
I/O Cache
(Buffers with
MESI state info)
I/O Component
I/O Component
I/O Component
230
235
240

Fig. 2

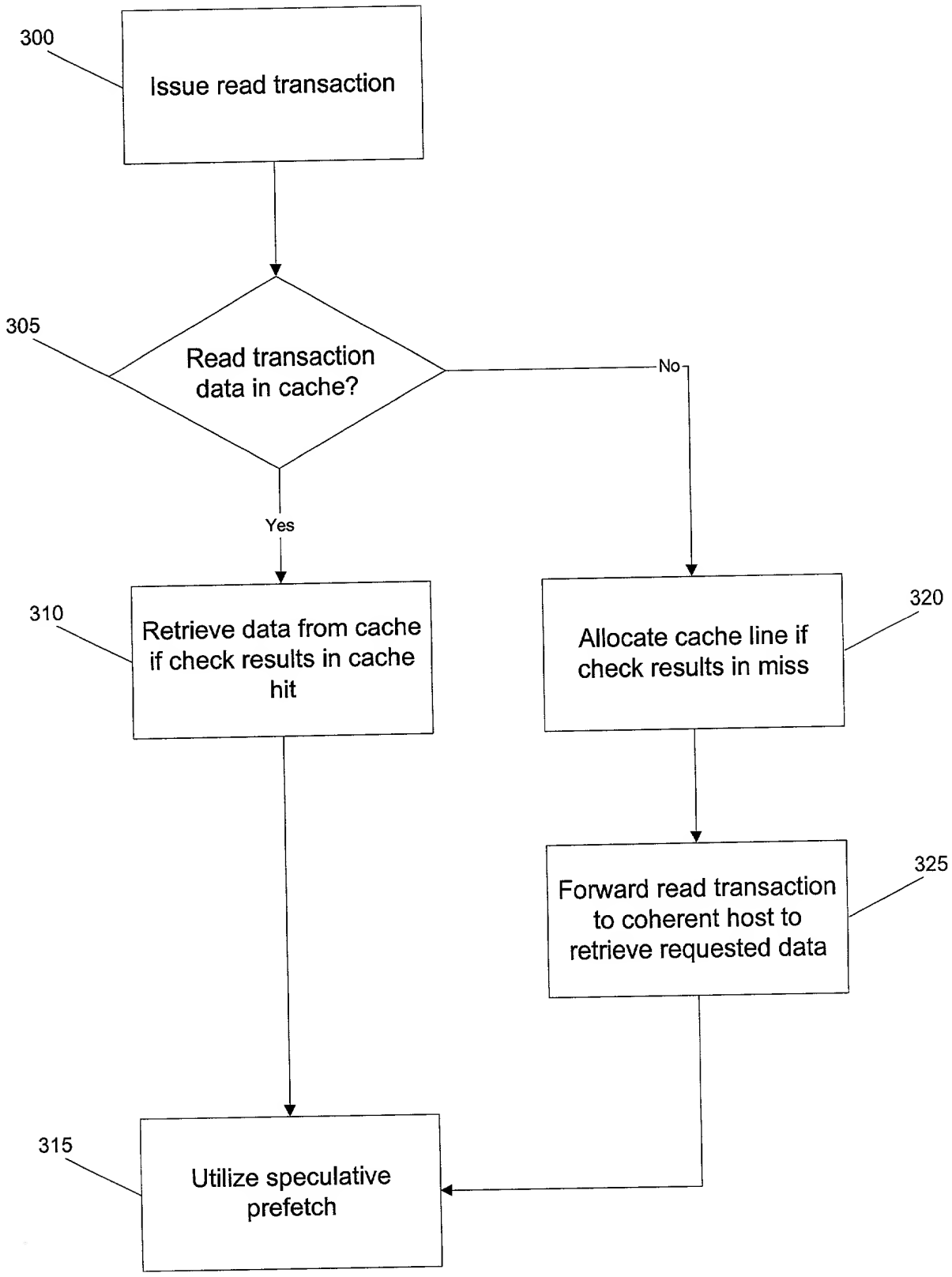
300
Issue read transaction
305
Read transaction data in cache?
No
Yes
310
Retrieve data from cache if check results in cache hit
320
Allocate cache line if check results in miss
325
Forward read transaction to coherent host to retrieve requested data
315
Utilize speculative prefetch

Fig. 3

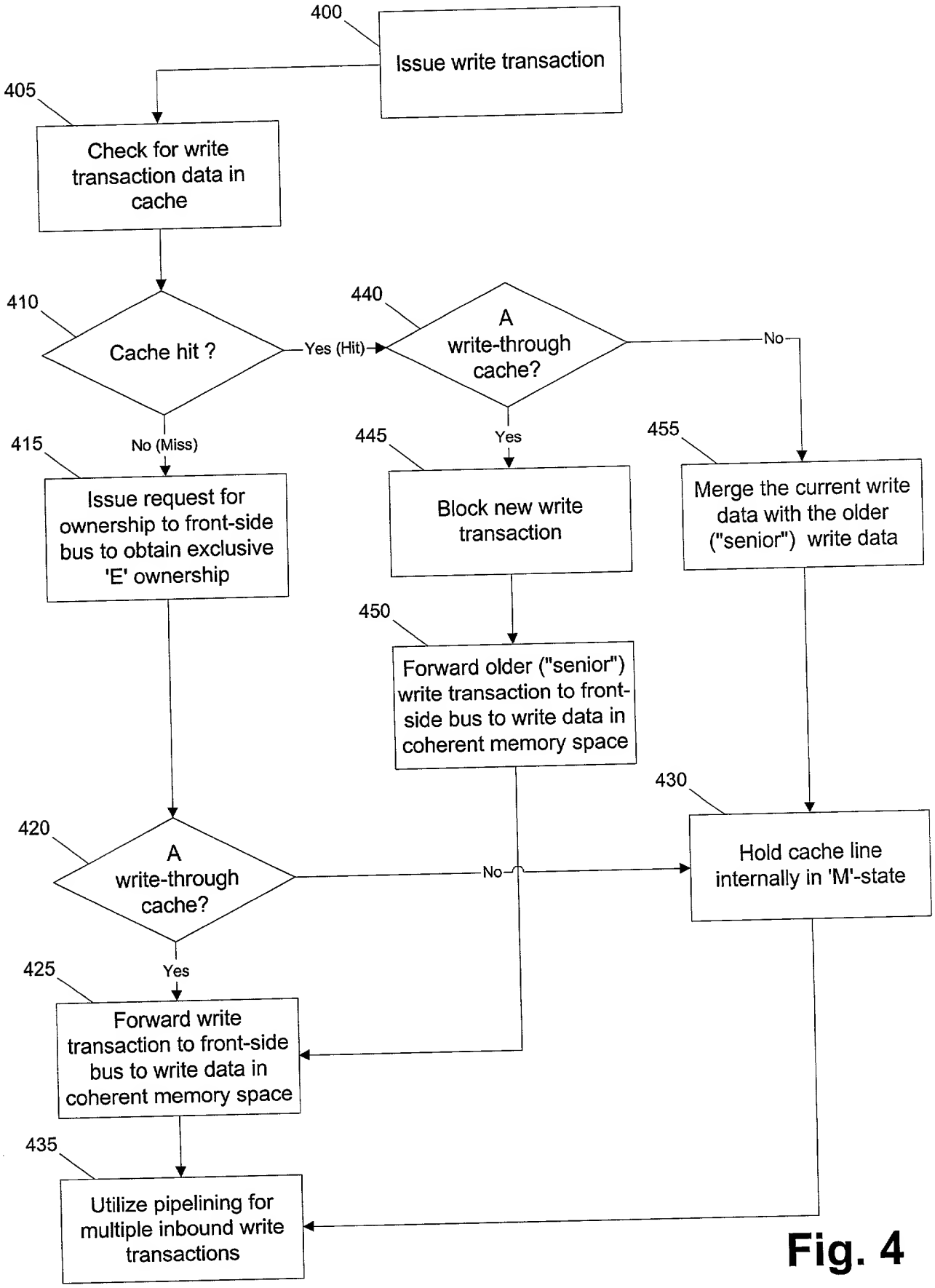
400
Issue write transaction
405
Check for write transaction data in cache
410
Cache hit ?
Yes (Hit)
440
A write-through cache?
No
No (Miss)
415
Issue request for ownership to front-side bus to obtain exclusive 'E' ownership
Yes
445
Block new write transaction
455
Merge the current write data with the older ("senior") write data
450
Forward older ("senior") write transaction to front-side bus to write data in coherent memory space
430
Hold cache line internally in 'M'-state
420
A write-through cache?
No
Yes
425
Forward write transaction to front-side bus to write data in coherent memory space
435
Utilize pipelining for multiple inbound write transactions

Fig. 4